March 9, 1998
GFK-0702Y

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: **IC693 CPU Modules**
IC693CPU311-AB
IC693CPU313S
IC693CPU323S
IC693CPU331-CC

Introduction

This document contains information about the above CPU modules that is not currently available in any other publication. (However, this information will be added to applicable publications when they are next revised.) Therefore, it is suggested that this document be saved and stored with the rest of your PLC documentation.

Subjects covered in this document are the new Demko labeling, new CPU firmware release 8.20, and carry-over information about previous CPU firmware release 8.0.

Demko Labeling for CPU331

The CPU331 module has been granted Demko Agency approval and will be labeled accordingly.

Functional Compatibility of New Firmware (8.20)

This new feature, break-free SNP, is compatible with existing SNP Master Units such as computers running PLC programming software, Programmable Coprocessor Modules, etc. In a few applications, primarily where a combination of multi-drop SNP communications and very short PLC sweep times are used, users may desire, for performance reasons, to disable the feature. This subject is covered in the section, "Disabling the Break-Free SNP Feature."

New Firmware Release

The following information applies to the release of CPU firmware Version 8.20, which provides a new feature called "break-free SNP".

Catalog Number Changes

When a product undergoes a change, its catalog number's revision letter, or letters, are changed to reflect this. This enables users to determine, from the catalog number on the product's label, what features and capabilities a particular product has. For example, for

the firmware change covered by this document, the IC693CPU311 module's revision letters were changed from AA to AB. The following table contains the catalog number changes to the applicable CPU modules for this firmware upgrade.

New Catalog Numbers for Firmware Version 8.20	Previous Catalog Numbers Replaced
IC693CPU311-AB	IC693CPU311-P, R, S, T, U, V, W, X, Y, Z, AA
IC693CPU313S	IC693CPU313E, F, G, H, J, K, L, M, N, P, R
IC693CPU323S	IC693CPU323F, G, H, J, K, L, M, N, P, R
IC693CPU331-CC	IC693CPU331Z, AA, AB, BB

Current Hardware and Firmware Numbers

The information in the following chart documents the current revision levels of the hardware (circuit boards) and firmware (EPROMs) used in these CPUs.

CPU Catalog Number	Board Identification	Board Revision	EPROM Label	EPROM Location
IC693CPU311-AB	BC3C2	44A731725-G01R02 or later	395-027L8.20	U8
IC693CPU313S	BC3C2	44A731725-G01R02 or later	395-018L8.20	U8
IC693CPU323S	BC3D2	44A731730-G01R04 or later	395-019L8.20	U8
IC693CPU331-CC	CP3A3	44A737299-G01R04 or later	395-045C8.20	U35

Upgrading to Firmware Version 8.20

If desired, older versions of the CPU modules can be upgraded to this new firmware version (8.20) by the installation of the correct firmware chip. Upgrade kits may be purchased that contain new firmware chips, installation instructions, and update labels. To order an upgrade kit, select the correct number for your CPU from the following table:

CPU Model	Upgrade Kit
IC693CPU311	44A731233-G14
IC693CPU313	44A731249-G10
IC693CPU323	44A735538-G10
IC693CPU331	44A731232-G14

GFK-0702Y *March 9, 1998*

Documentation

For detailed information on the CPUs covered in this document, refer to the manuals listed below. Note that all of these manuals are included in a PLC Publications CD ROM, which may be ordered by specifying catalog number IC690CDR002.

GFK-0356, IC693 Programmable Controller Installation Manual

GFK-0467, IC693 Programmable Controllers Reference Manual

GFK-0466, IC693 Programming Software User's Manual

Operational Notes

Upgrading Firmware EPROM

Users desiring to upgrade a CPU to the new firmware version should be aware that the user program, configuration, CPU ID (used for SNP communications), and status tables will automatically be cleared from memory when the CPU's firmware EPROM chip is changed. Therefore, before changing the firmware chip, a user should make a backup copy of the PLC's entire program folder, which consists of the user program, configuration, and status tables, so that they can be restored after the upgrade. Note that after restoring the program folder, the CPU ID must be set separately using IC641 programming software or the Hand-Held Programmer (HHP) .

Ethernet Interface Module Compatibility

All IC693 Ethernet Interface (IC693CMM321) modules used with firmware release 6.5 or later of the IC693 PLC should be updated to release 1.10 or later of the IC693CMM321. IC641 TCP/IP Ethernet software requires both CPU release 6.5 or later and IC693CMM321 release 1.10 or later.

During a RUN MODE (ALT-S) STORE of a large program block (greater than 14 Kbytes). the Ethernet Interface module may time out, causing communications to fail. Changing the Communications Window to Run-to-Completion mode, or storing the program in stop mode, will allow the Store to take place successfully.

FIP Bus Controller (FBC) Compatibility

The FBC version 3 or later is required for release 8.00 of the IC693 CPU firmware.

Memory Clear for the CPU331 Module

This paragraph documents the addition of "Memory Clear" connections to the CPU331 module. In general, CPU RAM memory is backed up by a battery on the Power Supply module. Additional backup is provided by a high-capacity capacitor, called a "supercap," on the CPU's circuit board. If it is desired to clear CPU memory in the CPU331 module, perform the following steps: (1) Unplug the CPU module from the PLC baseplate. This disconnects CPU memory from the backup battery located in the Power Supply module. (2) Connect a jumper for a few seconds across

the two connection pads, marked Mem. Clr, on the back of the CPU module. This discharges the supercap and clears RAM memory. (3) Remove the jumper before installing the module in the PLC.

New Features and Functionality

Break-Free SNP Feature

The purpose of this feature is to improve serial communications when modems are used. Break-free SNP simplifies modem communications with Series 90-30 PLCs by eliminating the requirement for a serial break at the start of each SNP and SNP-X session. Consequently, modem pairs that alter the timing or characteristics of breaks fromSNP/SNP-X masters may be used successfully.

Break-free operation is completely transparent to the user. When normal breaks are received,SNP/SNP-X communications are identical to previous firmware releases. When Attach and X-Attach messages are received, these are also recognized without a preceding break. Modified breaks (for example, breaks transformed to a single ASCII NUL character with or without a framing error) are ignored.

The break-free SNP feature requires data rates of 1200 bps (baud) and higher. Breaks are required at 300 and 600 bps. The PLC's auto-baud feature also requires breaks. Auto-baud permits Series 90-30 CPUs with no stored configuration to communicate at either 9,600 bps or 19,200 bps, odd parity, and one stop bit. Note that auto-baud is incompatible with modem communications because a stored configuration is required to set the serial port for no parity.

Disabling the Break-Free SNP Feature

For most applications, the impact of this feature on PLC sweep time will be negligible. However, the impact may be unacceptable for certain applications, particularly those using multi-drop SNP communications and very short PLC sweep times. In the case of multidrop SNP communications, all slave units must examine every received message, which may increase sweep time to an unacceptable value. A new COMMREQ command, described below, is provided to disable break-free SNP and eliminate its effect on PLC sweep time.

New Communications Request (COMMREQ) Commands

Disable Break-Free SNP Slave Operation: 7004

Available in slave mode only. This local command disables the break-free SNP feature in Series 90-30 CPU firmware version 8.20 (and later versions when they become available). Once disabled by this COMMREQ, break-free SNP remains disabled until the next time the PLC is power cycled, or until COMMREQ command 7005 is executed.

The COMMREQ that sends this command may be executed on the first PLC sweep.

If the COMMREQ instruction executes successfully, its fault output (FT) stays at logic 0, and its status word is set to logic 1. If the instruction does not execute successfully, or if the COMMREQ status word location specified in words 3 and 4 of the

command block is not a valid %R, %AI, or %AQ reference, its fault output is set to logic 1, and one of the following values will be written to its status word:

010Ch	WAIT-mode COMREQ is not permitted; must use NOWAIT
020Ch	Command not supported; the port is either not configured as an SNP slave, or does not support break-free operation

Sending this command when break-free SNP is already disabled has no effect; however, the COMMREQ status word will be set to 1 indicating success. Sending this command to a PLC CPU's built-in serial port that does not support break-free SNP will set the fault output of the COMMREQ.

COMMREQ 7004 Parameters:

SYSID:	**IC693CPU311, IC693CPU313, IC693CPU323:**	0	(0000)
	IC693CPU331, IC693CPU341:	1	(0001)
Task		00031	(001F)

Example of COMMREQ 7004 Command Block:

Memory Location	Memory Contents: Decimal (Hex)	Description
Word 1	00001 (0001)	SNP Data Block Length
Word 2	00000 (0000)	NOWAIT Mode
Word 3	00008 (0008)	Status Word Memory Type (%R)
Word 4	00000 (0000)	Status Word Address minus 1 (Register 1)
Word 5	00000 (0000)	Not used
Word 6	00000 (0000)	Not used
Word 7	07004 (1B5C)	SNP Command Number: Disable break-free SNP

Enable Break-Free SNP Slave Operation: 7005

Available in slave mode only. This local command enables the break-free SNP feature in Series 90-30 CPU firmware version 8.20 and later.

Because break-free SNP is enabled by default when the PLC is powered on, this command has no effect unless command 7004 (Disable Break-Free SNP) was previously executed. If a communications session is in progress when this command is executed, communications will continue and detection of no-break Attach/XAttach messages will begin when the current session is ended by a link-idle time-out.

The COMMREQ that sends it may be executed on the first PLC sweep.

If the COMMREQ instruction executes successfully, its fault output (FT) stays at logic 0, and its status word is set to logic 1. If the instruction does not execute successfully, or if the COMMREQ status word location specified in words 3 and 4 of the

command block is not a valid %R, %AI, or %AQ reference, its fault output is set to logic 1, and one of the following values will be written to its status word:

010Ch	WAIT-mode COMREQ is not permitted; must use NOWAIT
020Ch	Command not supported; the port is either not configured as an SNP slave, or does not support break-free operation

Sending this command when Break-free SNP is already enabled has no effect; however, the COMMREQ status location will be set to 1, indicting success. Sending this command to a PLC CPU built-in serial port that does not support break-free SNP will set the fault output of the COMMREQ.

COMMREQ Parameters:

SYSID:	**IC693CPU311, IC693CPU313, IC693CPU323:**	0	(0000)
	IC693CPU331, IC693CPU341:	**1**	**(0001)**
Task		00031	(001F)

Problems Resolved by This Release (Ver. 8.20)

The break-free SNP feature makes it possible to carry out SNP communications using modems that alter the normal SNP break timing or characteristics.

Problems Resolved by Release 8.00

ALT-S RUN MODE STORE of Periodic Subroutine

An Alt-S RUN MODE STORE should not be used to add or delete a periodic subroutine. This operation is now rejected in release 8.00 (rather than resulting in a PLC Watchdog fault). Note, however that editing an existing periodic subroutine with ALT-S in RUN mode is allowed.

HHP Write to Flash or EEPROM with IC641 Programmer Connected

When using the HHP (Hand Held Programmer) to write the program currently in memory into permanent storage (Flash or EEPROM), IC641 programming software must not be connected at the same time through other serial ports on the CPU351/352. Otherwise, incorrect data could be placed into the Flash or EEPROM area. To correctly store to Flash or EEPROM, either use IC641 programming software, or disconnect IC641 programming software while using the HHP to perform this function. This problem is fixed in release 8.00.

Restrictions and Open Problems

None